CLAIMS

1. A semiconductor component comprising:

a substrate having a surface;

a channel region located in the substrate;

a non-electrically conductive region substantially located below a substantially planar plane defined by the surface of the substrate;

a drift region located in the substrate and between the channel region and the non-electrically conductive region; and

an electrically floating region located in the substrate and contiguous with the non-electrically conductive region.

2. The semiconductor component of claim 1 wherein the channel region, the non-electrically conductive region, the drift region, and the electrically floating region are located at the surface of the substrate.

3. The semiconductor component of claim 1 wherein the electrically floating region is located between the drift region and the non-electrically conductive region.

4. The semiconductor component of claim 3 wherein the channel region, the non-electrically conductive region, the drift region, and the electrically floating region are located at the surface of the substrate.

5. The semiconductor component of claim 4 wherein a portion of the electrically floating region at the surface of the substrate is located between a portion of the drift region at the surface of the substrate and a portion of the non-electrically conductive region at the surface of the substrate.

6. The semiconductor component of claim 3 wherein the electrically floating region is located only between the drift region and the non-electrically conductive region.

7. The semiconductor component of claim 1 wherein the electrically floating region is located underneath the non-electrically conductive region.

8. The semiconductor component of claim 7 wherein the electrically floating region is located only underneath the non-electrically conductive region.

9. The semiconductor component of claim 1 further comprising:

a drain region in the substrate;

wherein:

the non-electrically conductive region is located between the drain region and the channel region; and

the electrically floating region is located between the non-electrically conductive region and the drain region.

10. The semiconductor component of claim 9 wherein the channel region, the non-electrically conductive region, the drift region, the electrically floating region, and the drain region are located at the surface of the substrate.

11. The semiconductor component of claim 1 wherein the electrically floating region is located between the non-electrically conductive region and the channel region and is located underneath the non-electrically conductive region.

12. The semiconductor component of claim 11 wherein the channel region, the non-electrically conductive region, the drift region, and the electrically floating region are located at the surface of the substrate.

13. The semiconductor component of claim 1 wherein the channel region is electrically isolated from a portion of the substrate located underneath the channel region.

14. The semiconductor component of claim 1 wherein the channel region is electrically coupled to a portion of the substrate located underneath the channel region.

15. The semiconductor component of claim 1 wherein the non-electrically conductive region comprises a trench in the substrate.

16. The semiconductor component of claim 15 wherein the non-electrically conductive region comprises a dielectric material in the trench.

17. The semiconductor component of claim 1 further comprising:

a gate electrode over the surface of the substrate,

wherein:

the channel region is located at least partially under the gate electrode;

the drift region is located under the gate electrode; and

the electrically floating region is located under the gate electrode.

18. The semiconductor component of claim 17 wherein:

the electrically floating region has a doping type;

the drift region has an other doping type different from the doping type of the electrically floating region and is located under the electrically floating region, and

a portion of the substrate has the doping type of the electrically floating region and is located under the drift region and under the electrically floating region.

19. The semiconductor component of claim 18 wherein the electrically floating region is located under the non-electrically conductive region.

20. The semiconductor component of claim 18 wherein the non-electrically conductive region is located under the gate electrode.

21. The semiconductor component of claim 1 wherein:

the electrically floating region has a doping type;

the drift region has an other doping type different from the doping type of the electrically floating region and is located under the electrically floating region, and

a portion of the substrate has the doping type of the electrically floating region and is located under the drift region and under the electrically floating region.

22. The semiconductor component of claim 1 wherein:

the electrically floating region comprises a first portion and a second portion;

the first portion of the electrically floating region is located underneath the non-electrically conductive region; and

the second portion of the electrically floating region is located at the surface of the substrate between a portion of the drift region at the surface of the substrate and a portion of the non-electrically conductive region at the surface of the substrate.

23. The semiconductor component of claim 22 wherein the first portion of the electrically floating region is separate from the second portion of the electrically floating region.

24. An integrated circuit comprising:

a semiconductor substrate having a surface, a portion of the semiconductor substrate having a first doping type;

a channel region located in the semiconductor substrate, having the first doping type, and located over the portion of the semiconductor substrate;

a non-electrically conductive region substantially located below a substantially planar plane defined by the surface of the semiconductor substrate and located over the portion of the semiconductor substrate;

a drift region located in the substrate, located between the channel region and the non-electrically conductive region, located between the portion of the semiconductor substrate and the non-electrically conductive region, and having a second doping type different from the first doping type; and

an electrically floating region located in the substrate, located between the non-electrically conductive region and the drift region, located between the non-electrically conductive region and the channel region, located over the portion of the semiconductor substrate and the drift region, and having the first doping type.

25. The integrated circuit of claim 24 further comprising a gate electrode located over the portion of the semiconductor substrate, the channel region, the non-electrically conductive region, the drift region, and the electrically floating region.

26. The integrated circuit of claim 25 further comprising:

a drain region located in the semiconductor substrate,

wherein:

the non-electrically conductive region is located between the drain region and the channel region.

27. The integrated circuit of claim 26 wherein the channel region, the non-electrically conductive region, the drift region, and the electrically floating region are located at the surface of the semiconductor substrate.

28. The integrated circuit of claim 27 wherein a portion of the electrically floating region at the surface of the semiconductor substrate is located between a portion of the drift region at the surface of the semiconductor substrate and a portion of the non-electrically conductive region at the surface of the semiconductor substrate.

29. The integrated circuit of claim 28 wherein:

the channel region has a first doping concentration; and

the electrically floating region has a second doping concentration less than the first doping concentration.

30. The integrated circuit of claim 28 wherein the channel region is electrically isolated from the portion of the semiconductor substrate.

31. The integrated circuit of claim 28 wherein the channel region is electrically coupled to the portion of the semiconductor substrate.

32. The integrated circuit of claim 28 wherein the non-electrically conductive region comprises a trench in the substrate and a dielectric material in the trench.

33. The integrated circuit of claim 24 wherein the portion of the semiconductor substrate and the electrically floating region provide a double reduced surface field effect.

34. A method of manufacturing a semiconductor component comprising:

providing a substrate having a surface;

forming a non-electrically conductive region substantially located below a substantially planar plane defined by the surface of the substrate;

forming a drift region in the substrate;

forming a channel region in the substrate, the drift region located between the channel region and the non-electrically conductive region; and

forming an electrically floating region in the substrate and contiguous with the non-electrically conductive region.

35. The method of claim 34 wherein forming the channel region and forming the electrically floating region occur simultaneously with each other.